

Q11: The following serial data are applied to the flip-flop through the AND gates as indicated in Figure 11. Determine the resulting serial data that appear on the Q output. There is one clock pulse for each bit time. Assume that Q is initially 0 and that PRE and CLR are HIGH. Rightmost bits are applied first.

J_1 : 1010011

J_2 : 0111010

J_3 : 1111000

K_1 : 0001110

K_2 : 1101100

K_3 : 1010101

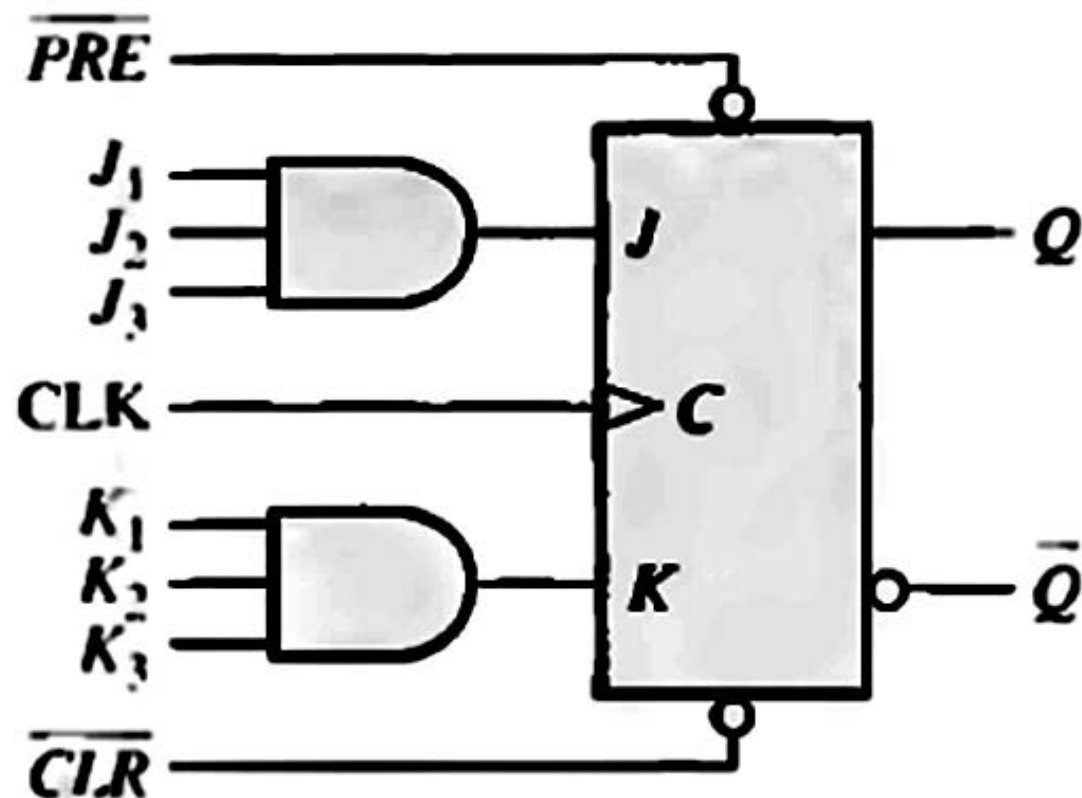
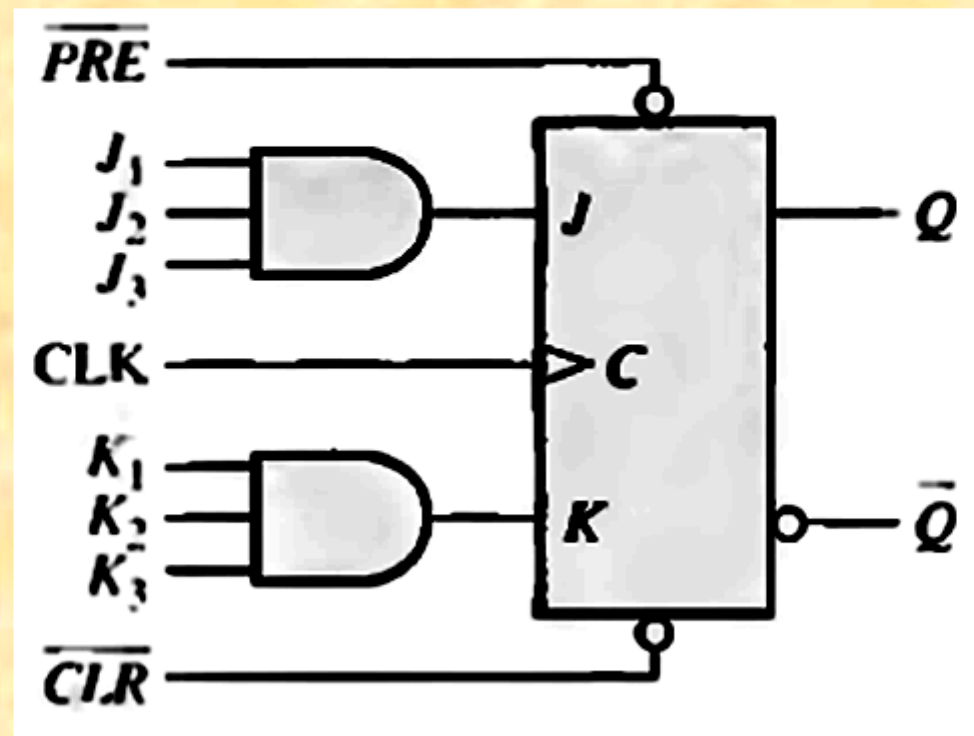
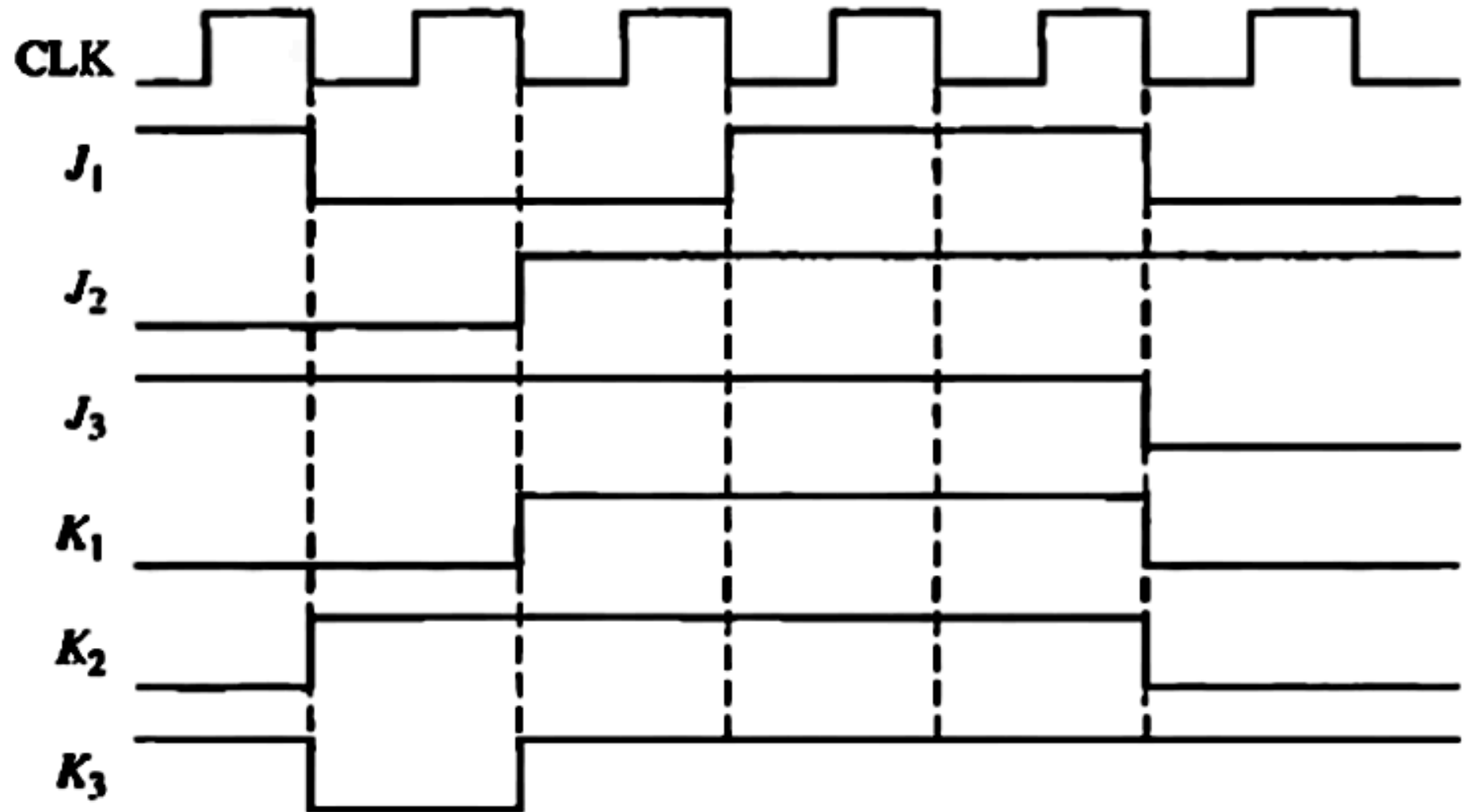


Figure (11)

Q12: For the circuit in Figure 12(a), complete the timing diagram in Figure 12(b) by showing the Q output (which is initially LOW). Assume PRE and CLR remain HIGH.



(a)



(b)